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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/753,766	12/29/2000	Udo Walterscheidt	2207/10124	3472

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KENYON & KENYON
Suite 600
333 W. San Carlos Street
San Jose, CA 95110-2711

EXAMINER	
O BRIEN, BARRY J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/753,766	WALTERSCHEIDT ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 5/03/04.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627, in further view of Bondi et al., U.S. Patent No. 5,881,277.

7. Regarding claims 1, 8 and 14, taking claim 1 as exemplary, Parady has taught a multi-threading processor, comprising:

a. A front-end module (14 of Fig.3),

b. An execution module (41 of Fig.3) coupled to said front end module,

c. A state module coupled to said front-end module and said execution module (see 48, 50, 110 of Fig.3). While not shown explicitly as a module, the state module's function, as described in the Applicant's specification, is encompassed by 48, 50, and 110 of Fig.3, which further shows the required interconnections,

d. A switch logic module (112 of Fig.3) coupled to said state module, wherein said switch logic module detects a long-latency event in a software thread and schedules a switch to another software thread during a latency of said long-latency event (see Col.3 lines 57-65).

8. Parady has not taught that the switch logic detects a mispredicted branch in a thread and schedules a switch to another thread during the latency of the mispredicted branch.

9. However, Bondi has taught that a branch misprediction event will result in large performance penalties, costing many cycles in order to fetch the correct path's instructions (see Col.1 lines 47-64). One of ordinary skill in the art would have recognized that increasing processor performance and throughput are of paramount concern to designers. Therefore, one of ordinary skill in the art would have found it obvious to modify Parady to also detect mispredicted branch events and schedule a switch to another software thread, in a manner similar to how Parady handles load instructions, in order to reduce the performance penalty suffered by the misprediction.

10. Claims 8 and 14 are nearly identical to claim 1. They differ in their lack of explicit hardware modules, but are both methods that encompass the same scope as claim 1. Therefore, claims 8 and 14 are rejected for the same reasons as claim 1.

11. Regarding claim 2, Parady in view of Bondi has taught a multi-threading processor as recited in claim 1, wherein the switch logic module detects a switching event (see Parady, Col.3 lines 57-65).

12. Regarding claim 3, Parady in view of Bondi has taught a multi-threading processor as recited in claim 2, wherein the switch logic module includes a cache miss indicator that is set when a cache miss is detected and reset when the switch is completed (see Parady, 114 of Fig.3 and Col.3 lines 57-64), but has not explicitly taught a mispredicted indicator that is set when a branch is mispredicted.

13. However, Bondi has taught a mispredicted signal (see Fig.2, and Col.6 lines 17-25) which is asserted when a branch is determined to have been mispredicted, and deasserted when the prediction is correct. Parady in view of Bondi, as shown above, has taught the detection of mispredicted branch events in order to minimize the performance penalty suffered by a misprediction. One of ordinary skill in the art would have recognized that the only way to detect a mispredicted branch is to execute the conditional branch instruction to get the result and compare it against the prediction. Therefore, one of ordinary skill in the art would have found it obvious to modify Parady to include the misprediction signal of Bondi in order to correctly detect a mispredicted branch.

14. Regarding claim 4, Parady in view of Bondi has taught a multi-threading processor as recited in claim 3, wherein the switch logic module includes an outstanding switch request

indicator that is set when the switching event does not require an immediate switch (see Parady, Col.1 lines 45-57 and Col.4 lines 53-62). For the case of a non-blocking load, there does not need to be an immediate switch. While not taught explicitly, there inherently must be a signal that is set to distinguish between blocking and non-blocking loads so that the processor knows if it can continue executing. This can be considered an outstanding switch request indicator because if it is a blocking load, this signal will be deasserted and not affect the normal thread switching operations.

15. Regarding claim 6, Parady in view of Bondi has taught a multi-threading processor as recited in claim 1, wherein the state module includes a pair of register files (48 and 50 of Fig.3) and a pair of IPs (110 of Fig.3).

16. Regarding claim 7, Parady in view of Bondi has taught a multi-threading processor as recited in claim 6, wherein the IPs are coupled to the front-end module and the register files are coupled to the execution module (see Fig.3).

17. Regarding claims 9 and 15, taking claim 9 as exemplary, Parady in view of Bondi has taught a method for concealing switch latency in a multi-threading processor as recited in claim 8, further comprising executing a switch to another software thread if the switching event requires an immediate switch (see Parady, Col.1 lines 45-57 and Col.4 lines 53-62).

18. Claim 15 is nearly identical to claim 9. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 15 is rejected for the same reasons as claim 9.

19. Claims 5, 10-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent No. 5,933,627, in further view of Bondi et al., U.S. Patent No.

5,881,277 as applied to claims 1-3 above, and further in view of Borkenhagen et al., U.S. Patent No. 6,567,839.

20. Regarding claims 5, 10 and 16, taking claim 5 as exemplary, Parady in view of Bondi has taught a multi-threading processor as recited in claim 4, but has not taught wherein the switch logic module includes a counter to schedule a switch based on a time quantum.

21. However, Borkenhagen has taught the scheduled switching between threads based on a time quantum and a countdown register to prevent threads from being inactive too long while processing a long-latency event (see Col.5 lines 50-57, Col.6 lines 32-35, and Col.18 lines 15-21). One of ordinary skill in the art would have recognized that inactive or stalled threads are wasting valuable processor cycles that could be spent processing other data. Therefore, one of ordinary skill in the art would have found it obvious to modify the multi-threaded processor as taught by Parady in view of Bondi to include the scheduled thread switching based on the a time quantum of Borkenhagen in order to force inactive threads to switch to new active threads, thus improving processor throughput and reducing wasted processor cycles.

22. Claims 10 and 16 are nearly identical to claim 5. While they differ in their parent claims, both claims encompass the scope of claim 5. Therefore, claims 10 and 16 are rejected for the same reasons as claim 5.

23. Regarding claims 11 and 17, taking claim 11 as exemplary, Parady in view of Bondi, in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 10, wherein the switch takes place "rapidly" (see Borkenhagen, Col.4 lines 38-41). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the switch has a latency of about 15 to about 20 clocks.

24. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make a switch with a latency of about 15 to about 20 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either the "rapidly" switching between threads taught by Borkenhagen or the claimed about 15 to about 20 clocks because both latencies perform the same function of providing a thread switch with minimal latency. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 11.

25. Claim 17 is nearly identical to claim 11. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 17 is rejected for the same reasons as claim 11.

26. Regarding claims 12 and 18, taking claim 18 as exemplary, Parady in view of Bondi, in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 11, wherein the time quantum can be customized according to a specific hardware configuration (see Borkenhagen, Col.18 lines 15-21, 36-38). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the time quantum is less than about 1,000 clocks.

27. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make the time quantum less than about 1,000 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected

Applicant's invention to perform equally well with either a "customized" time quantum or the claimed less than about 1,000 clocks because both quantums perform the same function of providing a time-out value to force a thread switch. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 12.

28. Claim 18 is nearly identical to claim 12. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 18 is rejected for the same reasons as claim 12.

29. Regarding claims 13 and 19, taking claim 19 as exemplary, Parady in view of Bondi in further view of Borkenhagen has taught a method for concealing switch latency in a multi-threading processor as recited in claim 12, wherein the time quantum can be customized according to a specific hardware configuration (see Borkenhagen, Col.18 lines 15-21, 36-38). Parady in view of Bondi in further view of Borkenhagen has not explicitly taught wherein the time quantum is about 200 clocks.

30. However, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to make the time quantum is about 200 clocks because the Applicant has not disclosed that doing so provides an advantage, is used for a particular purpose, or solves a stated problem. Furthermore, one of ordinary skill in the art would have expected Applicant's invention to perform equally well with either a "customized" time quantum or the claimed about 200 clocks because both quantums perform the same function of providing a time-out value to force a thread switch. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Bondi in further view of Borkenhagen to obtain the invention as specified in claim 13.

31. Claim 19 is nearly identical to claim 13. It differs only in its parent claim, but encompasses the same scope. Therefore, claim 19 is rejected for the same reasons as claim 13.

Response to Arguments

32. Applicant's arguments filed on 5/03/04 have been fully considered but they are not persuasive.

33. On page 6 of the present Amendment, the Applicant argues with respect to claims 1, 8 and 14:

> "*The office action asserts that Parady teaches an execution module coupled to a front end module. However, this is incorrect. The relied upon decode unit 14 is not coupled to the relied upon execution unit 41 (see Fig.3 of Parady).*"

34. However, Parady has taught an execution module (41 of Fig.3) coupled to a front-end module (14 of Fig.3). Although the path between the execution module to the front-end module of Parady includes other components, because the claim uses "comprising" language, rather than "consisting", the coupling of modules of Parady reads upon the claim limitation.

35. On page 6 of the present Amendment, the Applicant further argues with respect to claims 1, 8 and 14:

> "*The office admits that Parady does not teach the recited state module, and instead relies on a conflation of components including various register files 48, 50 and 110 as corresponding to the recited state module coupled to the front end module. However, none of the relied upon components 48, 50 or 110 are coupled to the relied upon decode unit 14 (see Fig.3 of Parady).*"

36. However, Parady has taught the registers files (48, 50 of Fig.3) as well as PA registers (110 of Fig.3) coupled to a front-end module (14 of Fig.3). Although the path between the register files and PA registers to the front-end module of Parady includes other components, because the claim uses "comprising" language, rather than "consisting", the coupling of modules of Parady reads upon the claim limitation.

37. On pages 6 and 7 of the present Amendment, the Applicant further argues with respect to claims 1, 8 and 14, in essence:

> *"In fact, Parady does not even mention and is not concerned with the problem of latency of mispredicted branches. Accordingly, there does not appear to be motivation to modify Parady to address this problem. ... In any event, the office action relies on Bondi for this missing teaching. However, the office action merely cites a portion of Bondi which identifies a problem in connection with a pipelined processor (Col.1 lines 47-64). The office action fails to identify any portion of Bondi which allegedly teaches or suggests modifying Parady in any way which might bear on the claims."*

38. The applicant is correct in noting that Parady or Bondi individually do not teach the motivation to combine the references, with Parady being directed towards switching threads on a cache miss, and Bondi being directed towards reducing the latency of a mispredicted branch. However, the Applicant is arguing the references individually, and not addressing the combination as a whole. The test for obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.

Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that

the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).

"Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).

"In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."

Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992).

39. Furthermore, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as shown in paragraphs 7-10 above, as well as in paragraphs 9-12 of the previous office action, Parady in view of Bondi has provided motivation for the combination of the references. In short, Parady has shown all of the limitations of exemplary claims 1, 8 and 14, except that it performs a thread switch upon detection of a long-latency event, namely a L2-Cache miss (see Parady, Col. 2 lines 18-24 and Col3 lines 57-65). Bondi has taught that mispredicted branches are long-latency events, and it is desirable to improve the speed of processing such events (see Bondi, Col.1 lines 47-64). Therefore, because Parady has taught the switching of threads upon detection of a long-latency event, and Bondi has taught that mispredicted branches are long-latency events, one of ordinary skill in the art would have found

it obvious to modify Parady to detect mispredicted branches and perform a thread switch in order to improve the throughput of the processor.

40. On pages 6 and 7 of the present Amendment, the Applicant further argues with respect to claims 1, 8 and 14, in essence:

> *"In fact, the technique discussed in Bondi for addressing the misprediction problem in a pipelined processor does not appear to have any bearing on the present claims. Applicants submit that if the Examiner more closely reviewed Bondi, he would discover that Bondi is directed to reducing the latency time of a mispredicted branch, and not to switching to another thread during such latency (e.g. see Col.16 lines 13-17)."*

41. The Applicant is correct in noting that Bondi is directed towards reducing the latency of a mispredicted branch rather than switching to another thread during said latency. However, again the Applicant is arguing the references individually, and not addressing the combination as a whole. The test for obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.

Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).

"Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).

"In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."

Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992).

42. On page 7 of the present Amendment, the Applicant further argues:

"*In view of the deficiencies in the references with respect to the independent claims, the dependent claims are not argued separately at this time. However, applicants note that the action contains many statements of what one skilled in the art might "recognize", without any reference to a teaching in the cited documents. If the rejections are maintained, applicants respectfully request that the Examiner identify a corresponding teaching in the references.*"

43. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Furthermore, the Applicant is arguing that motivation must be explicitly taught in the prior art of record. However, the test for obviousness is:

"whether the teachings of the prior art, taken as a whole, would have made obvious the claimed invention," In re Gorman, 933 F.2d at 986, 18 USPQ2d at 1888.

Subject matter is unpatentable under section 103 if it "'would have been obvious . . . to a person having ordinary skill in the art.' While there must be some teaching, reason, suggestion, or motivation to combine existing elements to produce the claimed device, it is not necessary that the cited references or prior art specifically suggest making the combination." In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988).

"Such suggestion or motivation to combine prior art teachings can derive solely from the existence of a teaching, which one of ordinary skill in the art would be presumed to know, and the use of that teaching to solve the same [or] similar problem which it addresses." In re Wood, 599 F.2d 1032, 1037, 202 USPQ 171, 174 (CCPA 1979).

"In sum, it is off the mark for litigants to argue, as many do, that an invention cannot be held to have been obvious unless a suggestion to combine prior art teachings is found in a specific reference."

Entire quote from In re Oetiker, 24 USPQ2d 1443 (CAFC 1992).

Conclusion

44. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

45. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

47. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
7/6/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100